Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a dicing region provided on a semiconductor substrate to separate a plurality of semiconductor chips each having a gate portion from each other;

a plurality of element isolation regions provided on a surface portion of the semiconductor substrate within the dicing region;

a plurality of first dummy patterns formed on a surface of the semiconductor substrate so as to correspond to intervals of the plurality of element isolation regions, respectively; and

a plurality of second dummy patterns formed above the semiconductor substrate within the dicing region so as to correspond to the plurality of first dummy patterns, respectively, wherein the plurality of first dummy patterns and the plurality of second dummy patterns at least partially assist in separation of the plurality of semiconductor chips from the semiconductor substrate.

2. (Original) The semiconductor device according to claim 1, wherein the dummy pattern has a wiring structure which is substantially equal to that of the gate portion.

3. (Canceled)

4. (Previously Amended) The semiconductor device according to claim 1, wherein the plurality of first dummy patterns each have a structure which is substantially similar to that of the first gate portion.

5. (Previously Amended) The semiconductor device according to claim 4, wherein the plurality of first dummy patterns and the gate portions each have a laminated structure including a gate oxide film, a polysilicon film, a WSi film, and a SiN film.

6. (Previously Amended) The semiconductor device according to claim 1, wherein the plurality of element isolation regions each have an STI structure.

7. (Previously Amended) The semiconductor device according to claim 1, wherein the plurality of first dummy patterns and the element isolation regions are arranged alternately to form a predetermined repetitive pattern.

8. (Previously Amended) The semiconductor device according to claim 1, wherein the plurality of second dummy patterns include at least protection films provided on the surface of the semiconductor substrate.

9. (Previously Amended) The semiconductor device according to claim 8, wherein the plurality of second dummy patterns include insulation films provided on the surface of the semiconductor substrate.

10. (Original) The semiconductor device according to claim 1, wherein the dummy pattern is formed along a dicing direction.

11. (Currently Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a plurality of semiconductor chips each having a gate portion on a semiconductor substrate; and

forming a projected dummy pattern in a dicing region between the semiconductor chips, wherein the projected dummy pattern assists in separating

the plurality of semiconductor chips from the semiconductor substrate in order to prevent a large waste from being caused by a crack during a dicing operation for separating the semiconductor chips from the semiconductor substrate.

12. (Previously Amended) The semiconductor device according to claim 1, wherein the dummy pattern is formed concurrently with formation of the gate portion.

13. (Original) The method according to claim 12, wherein the dummy pattern has a wiring structure which is substantially equal to that of the gate portion.